1. (Canceled)

2. (Canceled)

3. (Currently amended) A semiconductor imaging chip comprising:

an array of active pixel sensors arranged in rows and columns, each of said active pixels sensors having a respective active pixel sensor signal value and an active pixel sensor reset value;

an output terminal; and

a plurality of multiplexed column buffers, each of said plurality of multiplexed column buffers having a respective first plurality of input terminals coupled to a respective first plurality of said columns, a first of said plurality of multiplexed column buffers comprising:

first, second, third and fourth memory elements;

said first memory element adapted to store an active pixel sensor signal value for a first column of said array;

said second memory element adapted to store an active pixel sensor reset value for said first column of said array;

said third memory element adapted to store an active pixel sensor signal value for a second column of said array;

said fourth memory element adapted to and an active pixel sensor reset value for said second column of said array;

a differential gain amplifier having respective first and second input terminals and a respective output terminal;

said first input terminal of said differential gain amplifier being selectively coupled to one of said first and third memory elements;

said second input terminal of said differential gain amplifier being selectively coupled to one of said second and fourth memory elements; and

the output terminal of said differential gain amplifier being selectively coupled to said output terminal of said semiconductor imaging chip~~A semiconductor imaging chip in accordance with claim 1~~, wherein each of said plurality of multiplexed column buffers further comprises:

a multiplexed bus driver amplifier having respective input and output terminals;

fifth and sixth memory elements;

said fifth memory element being selectively coupled to said output terminal of said differential gain amplifier to store a corrected APS pixel signal value output for said first column of said array;

said sixth memory element being selectively coupled to said output terminal of said differential gain amplifier to store a corrected APS pixel signal value output for said second column of said array;

said input terminal of said multiplexed bus driver amplifier being sequentially coupled to said fifth memory and said sixth memory element so as to sequentially output a corrected APS pixel signal value for said first column of said array followed by a corrected APS pixel signal value for said second column of said array.

4. (Canceled)

5. (Canceled)

6. (Canceled)

7. (Previously presented) A multiplexed column buffer for use in a semiconductor imaging chip including an array of active pixel sensors arranged in rows and columns, said semiconductor imaging chip having an output terminal, said multiplexed column buffer comprising:

respective first, second, third, fourth, fifth, sixth, seventh, eighth, ninth, tenth, eleventh and twelfth switches;

respective first, second, third, fourth, fifth and sixth memory elements;

a differential gain amplifier having respective first and second input terminals and a respective output terminal;

a bus driver amplifier having respective input and output terminals;

said first switch coupling said first memory element to a first column of said array of active pixel sensors;

said second switch coupling said second memory element to said first column of said array of active pixel sensors;

said third switch coupling said third memory element to a second column of said array of active pixel sensors;

said fourth switch coupling said fourth memory element to said second column of said array of active pixel sensors;

said fifth switch coupling said first memory element to said first input terminal of said differential gain amplifier;

said sixth switch coupling said third memory element to said first input terminal of said differential gain amplifier;

said seventh switch coupling said second memory element to said second input terminal of said differential gain amplifier;

said eighth switch coupling said fourth memory element to said second input terminal of said differential gain amplifier;

said ninth switch coupling said fifth memory element to said output terminal of said differential gain amplifier;

said tenth switch coupling said sixth memory element to said output terminal of said differential gain amplifier;

said eleventh switch coupling said fifth memory element to said input terminal of said bus driver amplifier;

said twelfth switch coupling said sixth memory element to said input terminal of said bus driver amplifier; and

said output terminal of said bus driver amplifier being coupled to said output terminal of said semiconductor imaging chip.

8. (Canceled)

9. (Canceled)

10. (Canceled)

11. (Canceled)